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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/766,477	01/19/2001	Klan Teng Eng	TI-22944.2	2137

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EXAMINER

MITCHELL, JAMES M

ART UNIT	PAPER NUMBER
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2813

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	01/09/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary

Application No.

09/766,477

Applicant(s)

ENG ET AL.

Examiner

James M. Mitchell

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 11 October 2006.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 21-25 and 27-38 is/are pending in the application.
- 4a) Of the above claim(s) 29-36 and 38 is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 21-25, 27, 28 and 37 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 1/19/2001 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☐ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date _____.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application
- 6) ☐ Other: _____.

DETAILED ACTION

1. This office action is in response to applicant's appeal brief filed October 11, 2006.

Response to Amendment

2. Upon review of applicant's appeal brief, subsequent search and review of the prior art, examiner has come across both new and old references that anticipates or make obvious the claimed invention. As such, a new rejection has been made.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 21, 27, 28 and 37 are rejected under 35 U.S.C. 102(b) as being anticipated by Sowa (JP 06-267780).

5. Sowa (Fig 1) discloses:

(cl. 21, 37) a process of providing a high density module produced by a process comprising the steps of: providing a board/substrate that a component is mounted on and therefore a circuit board ("substrate" 5; Par. 0009) having a substantially planar top surface for connection to at least one integrated circuit package (1); providing an integrated circuit package having a pair of opposing major surfaces (e.g. Left and Right

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surfaces perpendicular to 2 & 22)¹ and at least one edge surface (22) disposed between said opposing major surfaces, one of said at least one edge surface having at least one electrical terminal (21) disposed thereon; and electrically connecting (e.g. solder, 4) said at least one electrical terminal on said at least one edge surface of said integrated circuit package to said top surface of said printed circuit board at an acute angle with said top surface of said printed circuit board (English Par. 0009, 0024);

(cl. 27, cont. 37) package connected at an acute angle between 30 and less than 90 degrees to said circuit board (Eng. Par. 0024);

(cl. 28) at least one edge surface is four edge surfaces (e.g. chip is rectangular).

6. Claims 21-25 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Cotues et al. (U.S. 5,239,447).

7. Cotues (Fig 4, 5) discloses:

(cl. 21) a process of providing a high density module produced by a process comprising the steps of: providing a circuit board (44) having a substantially planar top surface for connection to at least one integrated circuit package (40,); providing an integrated circuit package having a pair of opposing major surfaces (Regions near 40, 64) and at least one edge surface (region near 78) disposed between said opposing major surfaces, one of said at least one edge surface having at least one electrical terminal (48) disposed thereon; and electrically connecting (i.e. terminal in contact with items 24, 46) said at least one electrical terminal on said at least one edge surface of said

¹ Note that the phrase major surface is broad and per applicant's definition in his remarks filed September

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integrated circuit package to said top surface of said printed circuit board at an acute angle with said top surface of said printed circuit board;

(cl. 22) a step of electrically connecting at least two said integrated circuit packages to said circuit board at a said edge (i.e. electrical contact formed under edge; Fig 4);

(cl. 23) the step of disposing solder ball between said side surface terminal of said IC package and said top of said circuit board (Abstract; Col. 4, Lines 59-65);

(cl. 24) solder columns (Fig. 1, item 13) between said integrated circuit and said top of said circuit board;

(cl. 25, 27) further including the step of integrally attaching at least three tabs (pads, 4, 24, 54 etc. are projections used to identify/align package and therefore is a tab) package to said circuit board (cl. 27) said package is further defined as being connected at an acute angle between 30 and less than 90 degrees to said circuit board;

(cl. 28) wherein said at least one edge surface (i.e. surface crossing to parallel surfaces; shown in Fig 5) is four edge surfaces (Fig 2), each of said four edge surfaces disposed between said major surfaces (parallel surfaces (i.e. regions close to lines indicating 40,84) to form a closed package with said major surfaces.

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

8. Claims 21-23, 25 and 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Fujisawa (U.S 6,094,356).

9. Fujisawa (Fig 13,14,17) discloses:

(cl. 21, 37) a process of providing a high density module produced by a process comprising the steps of: providing a board/substrate (30) that a component is mounted on and therefore a circuit board having a substantially planar top surface for connection to at least one integrated circuit package (12); providing an integrated circuit package having a pair of opposing major surfaces (e.g. Left and Right surfaces almost vertical) and at least one edge surface (24) disposed between said opposing major surfaces, one of said at least one edge surface having at least one electrical terminal (22C) disposed thereon; and electrically connecting (Col. 10, lines 18-22) said at least one electrical terminal on said at least one edge surface of said integrated circuit package to said top surface of said printed circuit board at an acute angle with said top surface of said printed circuit board (e.g. less than 90 degrees);

(cl. 22) electrically connecting at least two integrated circuit packages (e.g. Fig . 17; Col. 6, Lines 54-61);

(cl. 23) disposing a solder ball (e.g. 32, 54) between terminal of package and board;

(cl. 25) attaching three tabs (e.g. pad o board providing electrical contact; Col. 10, Lines 18-22) to board;

(cl. 28) at least one edge surface is four edge surfaces (e.g. chip is rectangular).

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10. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

11. Claims 23 and 24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sowa (JP 06-267780).

12. Sowa discloses the elements stated in paragraph 5 of this office action, and further discloses a step of disposing solder (4) between said side surface terminal (21) of said IC package and said top of said circuit board (land, 3), but does not explicitly disclose that its solder is in the shape of a ball or column.

13. However, applicant has not disclosed that the claimed shape is for a particular unobvious purpose, produces an unexpected result or is otherwise critical². As such, the selection of the claimed dimension would have been obvious to one of ordinary skill in the art, since it has been held that that mere dimensional limitations are prima facie obvious absent a disclosure that the limitations are for a particular unobvious purpose, produce an unexpected result, or are otherwise critical. See, for example, *In re Rose*, 220 F.2d 459, 105 USPQ 237 (CCPA 1955); *In re Rinehart*, 531 F.2d 1048, 189 USPQ 143 (CCPA 1976); *Gardner v. TEC Systems, Inc.*, 725 F.2d 1338, 220 USPQ 777 (Fed. Cir. 1984), cert. denied, 469 U.S. 830, 225 USPQ 232 (1984); *In re Dailey*, 357 F.2d 669, 149 USPQ 47 (CCPA 1966).

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14. Claims 22 and 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Sowa (JP 06-267780) in combination with Fujisawa et al. (U.S. 6,094,356).

15. Sowa discloses the elements stated in paragraph 5 of this office action and further a tab (land, 3, formed on substrate), but does not disclose at least three tabs and at least two circuit packages.

16. Fujisawa (e.g. Fig. 17) discloses at least three tabs (e.g. pad on board in contact with solder) and at least two circuit packages.

17. It would have been obvious to one of ordinary skill in the art to form additional packages connected to the board of Sowa in order to provide increased density as taught by Fujisawa (Col. 6, Lines 54-61).

18. Claims 27 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cotues et al. (U.S. 5,239,447).

19. Cotues discloses the elements stated in paragraph 7 of this office action and further discloses a high-density module (Fig. 4) where its package is connected to its board less than 90 degrees ("non orthogonal"; Col. 2, Lines 64-65), but does appear to show explicitly that that its angle is between 30 and less than 90 degrees.

20. Because Cotues discloses the general conditions of applicant's invention, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form Cotues's chip between 30 and 90, since it has been held that where the general working conditions of a claim are disclosed in the prior art, discovering the optimum or

² Lack of criticality is further evidence by applicant's claim of different shapes (e.g. his claim 23 compared

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working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

21. Claims 24, 27 and 37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Fujisawa et al. (U.S. 6,094,356).

22. Fujisawa discloses the elements stated in paragraph 9 of this office action, but does not explicitly disclose a column shape solder, or that the package is connected to its board between 30 and less than 90 degrees.

23. With respect to the shape of its solder see paragraph 13 of this office action.

24. With respect to the angle that the package is connected, Fujisawa discloses the general conditions of applicant's invention. As such, it would have been obvious to one of ordinary skill in the art at the time the invention was made to form the chip's angle between 30 and 90 degrees, since it has been held that where the general working conditions of a claim are disclosed in the prior art, discovering the optimum or working ranges involves only routine skill in the art. *In re Aller*, 105 USPQ 233 (CCPA 1955).

Response to Arguments

25. Applicant's arguments with respect to claims have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

to claim 24.


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26. Any inquiry concerning this communication or earlier communications from the examiner should be directed to James M. Mitchell whose telephone number is (571) 272-1931. The examiner can normally be reached on M-F 8:00-4:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Carl Whitehead Jr. can be reached on (571) 272-1702. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Ex. Mitchell, J.D.
December 23, 2006


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